

Power Compiler

Automatic Power Management within Galaxy™ Implementation Platform

Overview

Power Compiler™ automatically minimizes power consumption at the RTL and gate level. Power Compiler performs automatic clock gating to reduce the power consumption. Driven by the design constraints, it performs simultaneous optimization for timing, power and area. With power intent defined by UPF (Unified Power Intent), it automatically inserts power management cells such as isolation, level-shifter, retention registers, power gates and always-on cells as needed. It also supports multi-threshold libraries for optimal leakage power optimization. Power Compiler is seamlessly integrated with the synthesis design flow and shares the same GUI, commands, constraints and libraries with the Design Compiler® and IC Compiler® tools.

Reducing power consumption is required in today’s semiconductor designs. Silicon technology advances have made it possible to pack millions of transistors switching at high clock speeds on a single chip. While these advances bring unprecedented performance to electronic products, they pose difficult power dissipation and distribution problems. These problems must be addressed, because consumers demand high performance along with longer battery life in addition to lower cost in computers, battery-operated systems, medical devices, telecommunications equipment and many high-volume consumer products.

Power Compiler provides fully automated and complete power synthesis:

- ▶ Single-pass multi-voltage optimization
- ▶ Automated implementation of advanced low-power methodologies
- ▶ Advanced clock-gating for optimal dynamic power savings
- ▶ Concurrent synthesis optimization for performance, area, leakage and test
- ▶ Fine-grain control over leakage optimization

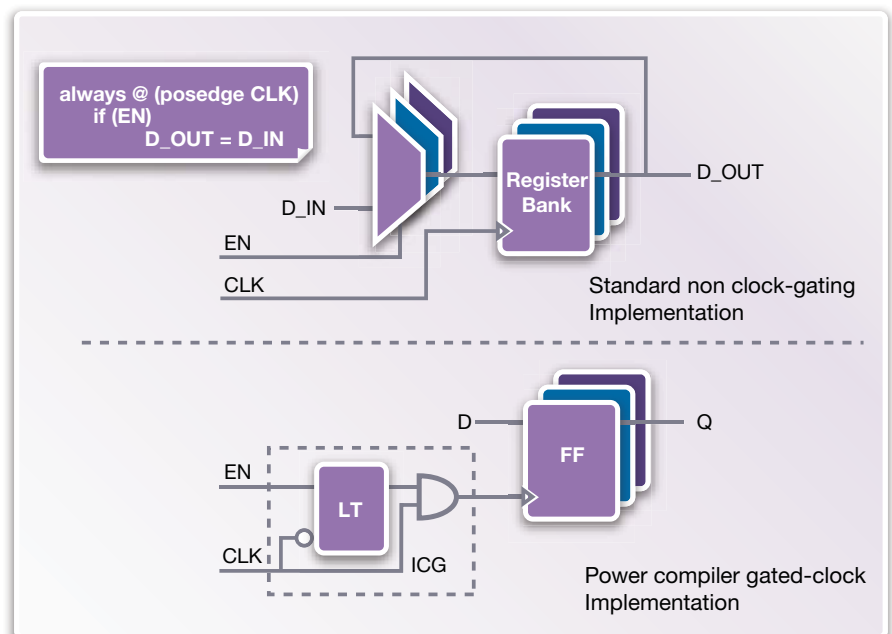


Figure 1: Power Compiler can perform clock gating at RTL or gate level

Power Compiler

Power Compiler™ automatically minimizes power consumption at the RTL and gate level. Power Compiler performs automatic clock gating to reduce the dynamic power consumption. Driven by design constraints, it performs simultaneous optimization for timing, power, area and test. It supports multi-threshold libraries for automatic leakage power optimization. It also offers concurrent multi-scenario synthesis, or multi-corner and multi-mode (MCMM) optimization. The concurrent optimization across all scenarios uses different libraries, referred to as multi-corners, or it can use different constraints (multi-modes). In conjunction with RTL or gate level representation of a design, Power Compiler uses UPF as input for implementation of advanced low power techniques such as power management cell insertion for multi-voltage designs that have shutdown and retention capabilities.

Power Management

A key to successful power management is automatic power reduction. This enables designers to meet their power budgets without adversely affecting their productivity or time to market. Power Compiler's push-button power reduction capabilities at the Register Transfer Level (RTL) and gate level are fully integrated with the Synopsys Galaxy™ Implementation Platform design synthesis and physical design flow.

Consistent Definition of Power Intent is Essential for Productive Automation

Early definition of power intent in the design flow enables downstream tasks in the process to be automated and driven by a consistent power specification. Power intent includes the specification of multiple voltage power domains, power shutdown

modes, isolation, voltage level shifting and retention behavior. Power intent is captured as a companion file to the RTL or gate level design using the standardized IEEE 1801 Unified Power Format (UPF).

Used in conjunction with the RTL or gate netlist of a design, UPF is used systematically throughout the design process to describe the design power intent. Power Compiler takes UPF input and automatically inserts the power management cells based on the power domain, strategy and state definitions.

Advanced Clock Gating

Synopsys' Power Compiler performs automatic clock gating without requiring any changes to the RTL source. This enables fast and easy trade-off analysis and maintains technology-independent RTL source. Power Compiler also performs clock gating of gate level designs. Clock gating is a common power reduction technique used manually in many power-critical designs. Power Compiler's clock gating is complementary to manual clock gating done at the block level. It gates the clocks of individual synchronous load-enable register banks instead of circulating the output back to the input when the load-enable condition is invalid. Power Compiler automates this

technique during the design elaboration phase, without requiring any additional effort from the design engineer. Power Compiler supports several advanced clock gating techniques including support for multi-stage, latency-driven, power-driven (using SAIF files), user-instantiated and XOR self-gating. When applicable, substantial power savings can be achieved – up to 70 percent or more – at the block level.

Power Compiler: Power Optimization

At the gate level, Power Compiler delivers further push-button power reduction. It delivers an average of 10 to 20 percent reduction in power during gate-level optimization without violating timing constraints. Based on the user's timing, power and area constraints, Power Compiler measures trade-offs between positive timing slacks, area and power and then delivers the lowest power-consuming design that meets timing constraints, while maintaining the area limit when specified by the user. The push-button power optimization at the gate level reduces the dynamic power as well as the leakage power, which is the majority of the power consumed when the device is in standby mode.

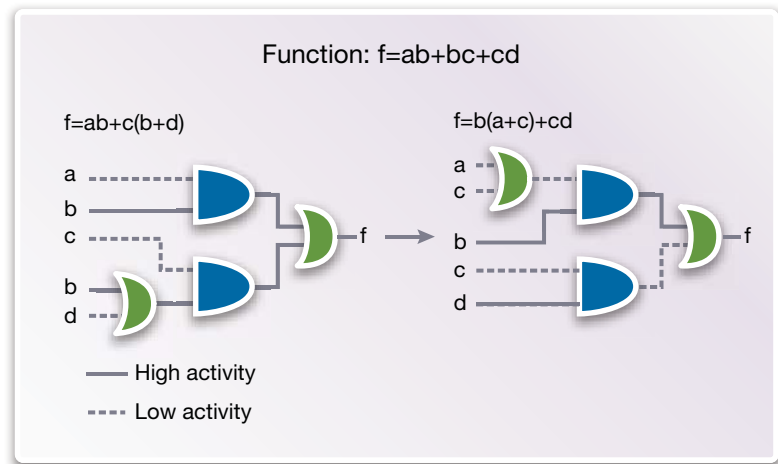


Figure 2: Factoring technique for reducing the circuit switching activity

Power Compiler offers fine-grain control of leakage optimization through the capability of assigning a limit to the number of low voltage threshold cells used – these type of cells offer higher performance but are also the most leaky cells in a library. It enables multi-corner and multi-mode (MCMM) optimization which is essential for accounting for various design scenarios concurrently such as performance, leakage, temperature inversion and functional modes. The concurrent optimization across all scenarios uses different libraries, referred to as multi-corners, or it can use different constraints (multi-modes). Power Compiler shares the same GUI, shell, and compile commands with Design Compiler and IC Compiler. It is fully integrated with Design Compiler and the existing design flow.

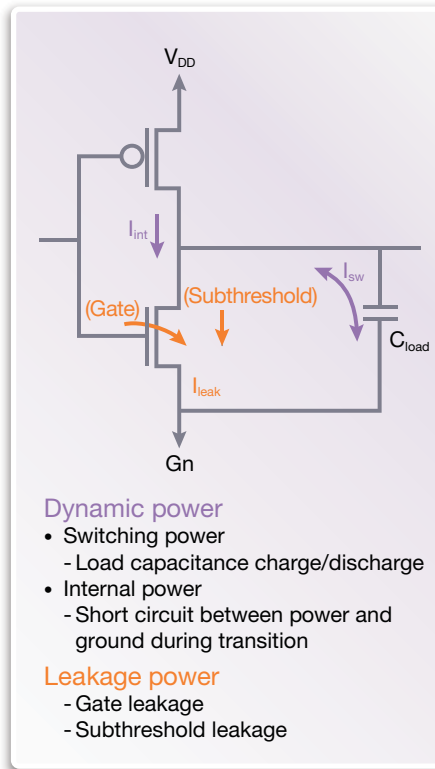


Figure 3: Power dissipation in CMOS design

Synopsys Advantage

The Synopsys Power Management Solution for the design flow gives designers a powerful arsenal of tools to optimize, estimate, analyze and manage today’s shrinking power budgets. Design engineers who are serious about providing power-efficient, cutting-edge technology to their customers will easily see the value in handling power problems early in the flow. By understanding a design’s power requirements at every phase of the design cycle, engineers will be able to produce high-performance, power-sensitive products without impacting cost or time to market.

For a complete directory of Synopsys’ available Power Solutions visit:
www.synopsys.com/galaxypower.