



## FPGA Design Solutions for Military and Aerospace Applications

- ▶ High Reliability
- ▶ Technology Independence
- ▶ High Performance Through Optimization
- ▶ Used in DO-254 Compliance
- ▶ High-Level RTL Synthesis
- ▶ Fast Debug and Verification

## Synopsys FPGA Implementation Solutions Provide Significant Advantages for Military and Aerospace Applications

As a hardware designer targeting military and aerospace applications you have special requirements that demand powerful, highly reliable design tools and methodologies. It is critical that tools used in the development of these applications not only understand the conditions under which the applications operate, but also the special development requirements needed to create them. Synopsys leverages its many years and wide range of design tool experience to deliver high-quality, high-performance and technology-independent solutions for FPGAs that will ultimately end up in space or other harsh operating environments. Synopsys FPGA design tools, verification tools, and methodologies comprehend the unique needs and parameters of MilAero and high reliability design applications and have been used in many successful projects, such as the Mars Rover.

*“Actel has a rich heritage of providing industry leading military and aerospace FPGAs and design solutions. Actel’s long and fruitful collaboration with Synopsys provides our military and aerospace customers with best-in-class FPGA synthesis and debug solutions.”*

### Jim Davis

Vice President of Software and Systems Engineering,  
Actel Corporation



Synopsys’ proven development process and widely used design tools can help you to meet your requirements without compromising safety or performance. Synopsys tools enable you to develop a reproducible requirements-driven design process that includes system specification, RTL coding, logic synthesis and verification. Designers use Synopsys’ FPGA design and verification tools for implementation of DO-254 processes to meet FAA standards and ensure the safety of airborne hardware.

### High Reliability Design Support

Several advanced optimization techniques have been incorporated into our FPGA design tools that address high-reliability applications such as Single Event Upset (SEU), Safe State Machines and support for RadHard and Radiation Tolerant FPGAs. These features may be easily enabled for an automated implementation of:

**TMR**—Synopsys solutions for Actel devices include the Triple Module Redundancy (TMR) method of handling SEUs. Combinatorial Cells (CC) with feedback are used in place of flipflops or latches. The TMR feature automatically implements each register in triplicate and then performs a “vote” to determine the register’s true state.

**Safe State Machine Encoding**—Synopsys FPGA design software allows you to specify an attribute that tells the tool to use safe state machine encoding algorithms to produce a highly reliable implementation of the state machine in your design.

**Automated Documentation**—The HDL Analyst tool, built in to Synopsys synthesis solutions, automatically produces highly readable schematics at both the RTL and gate level from your HDL source that may be used for code analysis and professional documentation of your design.

**Support for Legacy FPGA Devices**—The long life cycles associated with many MilAero applications demand that design software and FPGA parts be archived for potential future use. Synopsys offers archive licenses of software for this purpose and typically offers synthesis support for mature devices longer than is supported by FPGA vendor software.

### DO-254 Support

The RTCA/DO-254 standard enhances safety in airborne electronic systems and is comprised of five levels of stringency, levels A to E, which are based on the effect of the failure of the hardware upon an aircraft. Synopsys offers the Synplify® family of high-performance, technology-independent implementation & debugging solutions designed to aid DO-254 compliant processes for FPGA development. In addition, accurate functional verification versus initial requirements is a critical component of meeting DO-254 standards. A Synopsys verification flow, centered on the VCS® RTL verification solution coupled with the VMM (Verification Methodology Manual) methodology promote the creation, execution and measurement of a complete verification

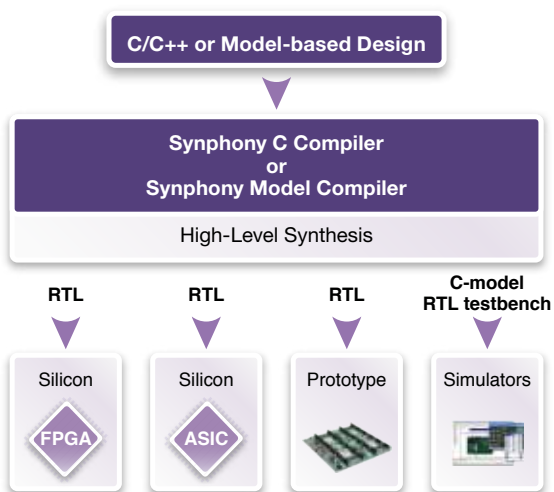
plan. Prototyping can be an important step in verifying DO-254 compliance and Synopsys provides a comprehensive FPGA-based prototyping solution that enables hardware-based verification for both ASIC and FPGA-based systems. These tightly integrated, easy to use products facilitate complete system debugging & early software development.

*“Designs targeted for military and aerospace applications require the highest level of quality and reliability. The combination of Xilinx Aerospace & Defense radiation tolerant FPGA family and Synopsys production-proven FPGA synthesis products offer designers not only the best performing devices, but more importantly, high reliability and quality.”*

**Amit Dhir**  
Sr. Director, Aerospace & Defense Business, Xilinx, Inc.

### High-Level Synthesis

Synopsys also provides a set of high-level synthesis (HLS) tools that achieve greater design and verification productivity from algorithm concept into silicon. Symphony C Compiler and Symphony Model Compiler provide optimized implementation paths from C/C++ and high-level, fixed-point models into RTL. Both products provide HLS optimization technologies that deliver high quality of results for FPGA and ASIC and enable rapid exploration of performance, power, and area tradeoffs. With Symphony, users can specify designs at a very high level of abstraction using C/C++ languages or IP model libraries, and then use the Symphony HLS compilers to create optimized RTL and testbenches for ASIC and FPGA, FPGA-based and virtual prototyping, and for verification using C or RTL.



**Synphony HLS provides higher DSP algorithm-to-silicon efficiency**



### RTL Verification and FPGA-Based Prototyping

Synopsys offers the VCS functional verification and debug verification environment allowing chip and system developers to find and fix critical design defects as early as possible and avoid schedule delays and production costs later. VCS working alongside the VMM methodology support a DO-254 compliant RTL verification solution.

The Synopsys FPGA-based prototyping solution enables pre-silicon software development and hardware/software co-verification of both subsystems and complete systems at near real-time speeds using real-world interfaces. Software development and system integration teams will benefit from improved productivity and a reduction in the overall product development schedule. The complete solution consists of HAPS® High-performance ASIC Prototyping System™ hardware supported by an integrated tool flow that includes Synplify® FPGA synthesis, Certify® design partitioning, and Identify® interactive debugging software. Synopsys’ FPGA-based prototyping solution is ideal for demanding verification environments where real-world interfaces and large test suites are essential.

*“Altera’s FPGAs and HardCopy ASICs address requirements for COTS-based solutions, providing military customers access to the latest commercially available technologies for the development of secure communications, electro-optic/IR, advanced sensor applications and electronic warfare. These solutions offer anti-tampering design security, end-of-life protection, military temperature support and quality and reliability levels for rugged environments. Together with Synopsys’ FPGA design tools, Altera’s programmable solutions enable military customers to develop highly reliable systems while achieving optimal results and managing technical risk.”*

**Amr El-Ashmawi**  
Sr. Business Unit Manager, Altera Corporation

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