

Eclipse Low Power Solution

Comprehensive Support for Advanced Low Power Design



Overview

The Synopsys Eclipse™ Low Power Solution provides a comprehensive, silicon-proven approach to low power design that is power-aware at every stage of the design cycle. The perfect alignment of technology, methodology, intellectual property, services and industry standards, the Eclipse Low Power Solution simplifies the deployment of advanced low power design techniques. The Eclipse Low Power Solution is built around support for industry standard IEEE 1801 Unified Power Format (UPF), the most widely adopted language to describe power intent. Spanning the entire design cycle, from early architectural and system-level analysis, to verification, RTL synthesis, test, physical implementation and signoff, the Eclipse Low Power Solution enables designers to achieve the fastest time-to-results (TTR) with the lowest risk.

The Low Power Challenge

Today's deep submicron semiconductor processes offer designers the ability to implement incredibly rich functionality even on small, inexpensive die. However, the resultant dynamic power dissipation arising from high frequency switching of the tens of millions of transistors to support this rich functionality directly impacts other critical product needs, including battery life, packaging and cooling costs, form factor and reliability. In addition, with the migration to 65 nm process geometries and below, leakage power becomes as problematic as dynamic power, and will eventually dominate as technology moves to 32nm process geometries and below.

- ▶ System-Level Concerns
 - Battery life
 - System cooling
 - Reliability
 - Packaging cost
 - Operating cost
 - Air-conditioning cost
 - New "Green" standards compliance
- ▶ Silicon-Level Concerns
 - More computing power
 - Limited power budget
 - Design complexity
 - Verification complexity
 - Testing and reliability
 - Schedule

In order to solve this challenge, designers must incorporate low power design techniques—addressing both dynamic and leakage power dissipation—throughout the design process. Low power design techniques will cause varying degrees of impact to implementation and verification flows, as well as impact to quality-of-results (QoR). Selecting the optimal low power design architecture is critical to attain the greatest power reduction at the lowest design impact.

Eclipse Low Power Solution

The Eclipse Low Power Solution (Figure 1) simplifies low power design and verification by combining and automating a wide array of advanced techniques, methodologies, and standards. The Eclipse Low Power Solution delivers leading-edge, silicon-proven, advanced low power technologies, built on support for industry-standard IEEE 1801 UPF. UPF-enabled tools include MVRC, VCS® with MVSIM, Design Compiler® Ultra, IC Compiler, DFTMAX, Formality®, and the PrimeTime® Suite.

Completing the solution are additional tools for low power design, including Innovator, CustomSim™, TetraMAX®, and PrimeRail, as well as DesignWare® IP, DesignWare® minPower Components and Synopsys Professional Services. The Eclipse Low Power Solution supports open methodologies, including those described in the “Low Power Methodology Manual” (LPMM), co-authored by Synopsys and ARM, and the “Verification Methodology Manual for Low Power” (VMM-LP), co-authored by Synopsys, ARM and Renesas.

Support for Advanced Low Power Techniques

The Eclipse Low Power Solution provides comprehensive support for the wide range of low power design techniques designers may adopt to achieve their low power goals. Figure 2 shows some of these techniques, and general industry adoption trends.

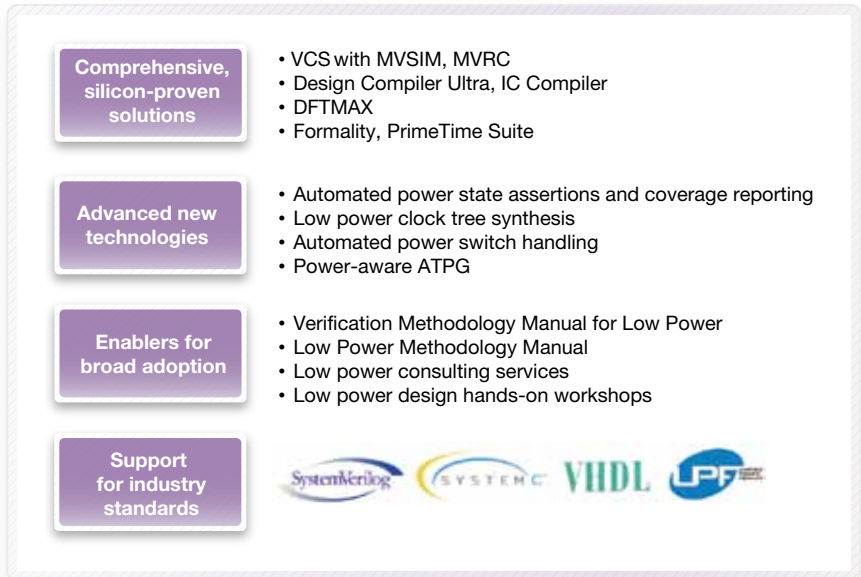


Figure 1: Eclipse Low Power Solution features and benefits

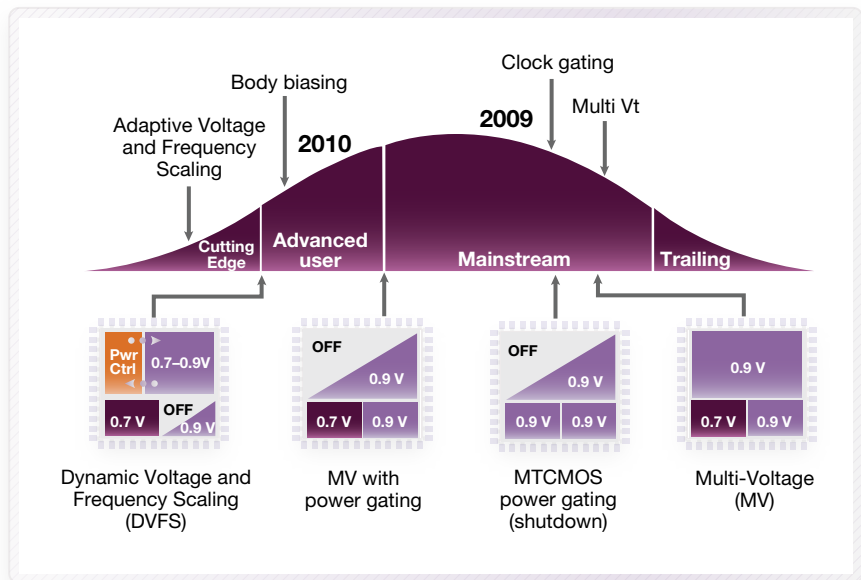


Figure 2: Adoption roadmap for advanced low power techniques

Advanced low power design techniques, such as MTCMOS power gating, multi-voltage, and dynamic voltage and frequency scaling (DVFS), force a major shift in how engineers create and verify chips. These techniques can dramatically reduce power consumption in deep submicron chips but have traditionally required ad-hoc, time-consuming, risk-prone, and

manual verification and implementation approaches. The Eclipse Low Power Solution combines a wide array of advanced techniques, methodologies, standards, and automation to simplify advanced low power design and verification. Table 1 characterizes some of the tradeoffs designers must consider when adopting low power design techniques.

Low power technique used	Dynamic power reduction	Static power reduction	Timing/area penalty	Verification impact	Implementation impact
Clock gating	Moderate	None	Minimal	Minimal	Minimal
Multi-Vt optimization	None	Moderate	None	None	Minimal
Multiple voltage islands	High	Moderate	Minimal	High	Moderate
MT-CMOS power gating	Minimal	Very high	Very high	Very high	Very high
Biasing: standby/active leakage	None	Minimal/moderate	Minimal	High	High
DVFS	Very high	Moderate	Very high	Very high	Very high

Table 1. Low power design technique, benefit, and impact

Conclusion

The Eclipse Low Power Solution delivers several new, advanced low power technologies. DesignWare® minPower Components provide reduced power for designs with significant datapath content by providing architectures specifically optimized for low power as well as additional optimizations, such as datapath gating, that are specifically targeted to reduce power along datapath. Enhanced automation for power switch insertion and optimization enables power planning exploration and “what-if” analysis using IR drop and area constraints, and In-Design Rail Analysis enhances

ease-of-use by providing for the verification of power meshes using PrimeRail signoff technology in the familiar IC Compiler environment for faster power mesh closure.

The Eclipse Low Power Solution is the industry’s most comprehensive suite of proven system-level, verification, implementation and signoff tools, intellectual property (IP), methodologies and services for low power chip development. The Eclipse Low Power Solution perfectly aligns Synopsys’ proven offerings from over 10 years of low power design leadership into a streamlined, easy-to-use low power workflow encompassing every phase

of the design process. As a result, the Eclipse Low Power Solution enables design teams to adopt advanced low power techniques while dramatically reducing time-to-results (TTR), reducing risk and ultimately delivering the highest quality silicon in the challenge to meet the most demanding power, area, speed and yield objectives.

For more information about the Synopsys Eclipse Low Power Solution, support services or training, please visit us on the web at www.synopsys.com or call 650.584.5000.

